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CHARACTERIZATION OF SILICON-GATE CMOS/SOS INTEGRATED CIRCUITS PROCESSED WITH ION IMPLANTATION

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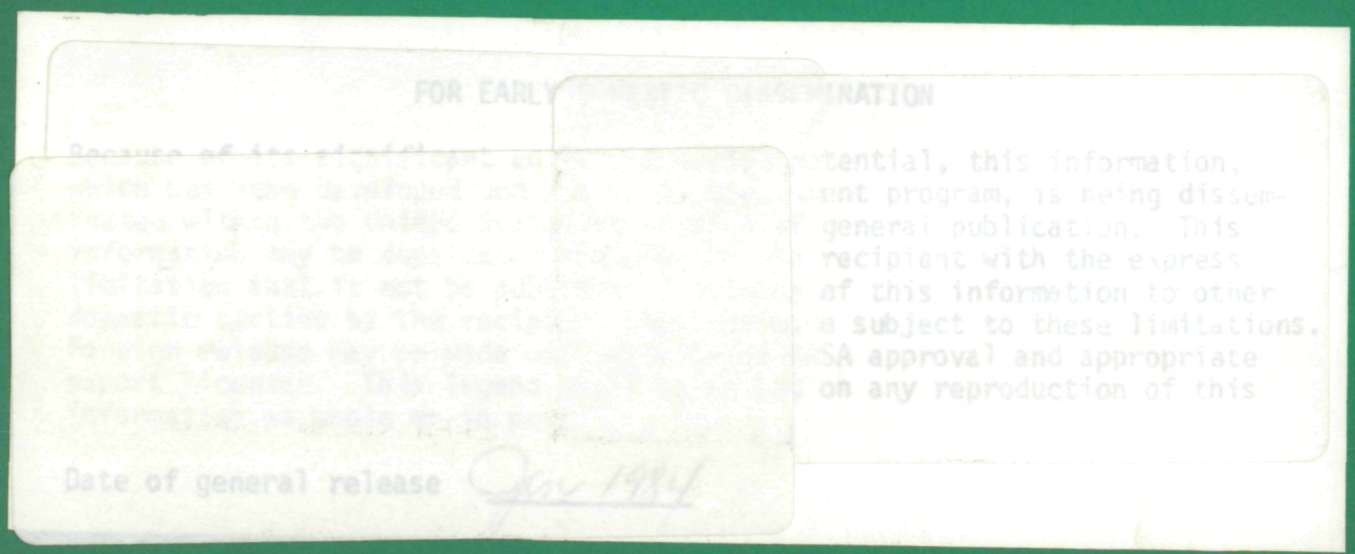
Solid State Technology Center
Somerville, NJ 08876

January 1982

Final Report for the period 1 September 1979
to 1 September 1980

Contract No. NAS8-31986



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Prepared for
George C. Marshall Space Flight Center
Marshall Space Flight Center, AL 35812

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SUMMARY

This Final Report on Contract NAS8-31986 describes the procedure used to generate MEBES masks and produce test wafers from the 10X Mann 1600 Pattern Generator Tape using existing CAD utility programs and the MEBES machine in the RCA Solid State Technology Center. The test vehicle used is the MSFC-designed SC102 Solar House Timing Circuit.

When transforming the Mann 1600 tapes into MEBES tapes, extreme care is required in order to obtain accurate minimum linewidths when working with two different coding systems because the minimum grid sizes may be different for the two systems. The minimum grid sizes are 0.025 mil for MSFC Mann 1600 and 0.02 mil for MEBES. Some snapping to the next grid is therefore inevitable, and the results of this snapping effect are significant when submicron lines are present. However, no problem was noticed in the SC102 circuit because its minimum linewidth is 0.3 mil (7.6 μm).

MEBES masks were fabricated and wafers were processed using the silicon-gate CMOS/SOS and aluminum-gate COS/MOS processing developed in the earlier phases of Contract NAS8-31986.

I. INTRODUCTION

The purpose of this project was to use the Manufacturing Electron Beam Exposure System (MEBES) mask-making equipment to generate a set of microcircuit masks from magnetic tape furnished by Marshall Space Flight Center (MSFC) and to process SOS and bulk technology versions of the circuit up to the metallization steps.

The data on the tape is in the Mann 1600 Pattern Generator data format which is 512 characters per record. The circuit is a MSFC-designed Solar Cell House Timing Circuit SC102 which is 162x131 mil with a minimum linewidth of 0.3 mil. Two sets of masks for use with two different process technologies are required for the circuit; one set (TCS221) is for the double-layer metal silicon-gate CMOS/SOS, and the other set (TCS261) is for the aluminum-gate COS/MOS bulk silicon.

RCA used the generated MEBES mask sets to fabricate the MSFC102 circuits using the silicon-on-sapphire (SOS) and bulk silicon technologies and using the RCA developed all-ion-implanted techniques for control of impurities. Both SOS and bulk silicon wafers were completed to the point of the first level of metallization, then shipped to MSFC with the necessary masks for completion of the devices at MSFC.

II. CONVERSION OF MANN TAPE TO MEBES TAPE

A. INTRODUCTION

In this section, the various steps used to generate the MEBES tapes for the MSFC102 circuits are discussed. The generation of masks from the MEBES tape was performed using the standard ETEC-supplied procedures and this part of the procedures is not covered in this report. The Mann 1600 tape supplied by MSFC included the various levels in a total of 20 files, shown in Table 1.

TABLE 1. FILES, MASK LEVEL, AND IDENTIFICATION IN NASA-SUPPLIED MANN 600 TAPE

File	Level	Identification or Function
		SOS TCS221
1	1	P-epi islands SOS
2	2	N-epi islands SOS
3	3	Poly definition SOS
4	4	N+ diffusion definition SOS
5	5	Contact definition SOS
6	6	First metal definition SOS or bulk
7	7	Intermetal oxide cut SOS or bulk
8	8	Second metal definition SOS or bulk
9	9	Passivation oxide cut SOS or bulk
10	10	P+ diffusion definition SOS
11	11	P & N epi islands (combining levels 1 & 2 together) SOS
		Bulk Silicon TCC261
12	1	P well bulk
13	2	P+ diffusion definition bulk
14	3	N+ diffusion definition bulk
15	4	Thick oxide cut bulk
16	5	Contact definition bulk
17	6	First metal definition SOS or bulk
18	7	Intermetal oxide cut SOS or bulk
19	8	Second metal definition SOS or bulk
20	9	Passivation oxide cut SOS or bulk

Note that levels 6 through 9 are common to both SOS and the bulk technology. Note also thet level 11 of the SOS mask set is a combination of levels 1 and 2.

The form of the information on the Mann 1600 tape was first transformed into the RCA DFL data format. The next steps were to generate a PLOT file, perform some editing, and finally generate a Versatec plot. The detailed steps are summarized below.

B. CONVERSION STEPS

1. Transform the Mann 1600 data to the DFL format and generate a DFL tape. The tape is named TCS221.DFL.
2. Load the TCS221.DFL tape into the IBM 370 TSO system.
3. Transform into a PLOT file using the command "SI TCS221 DFL AS SC102 PLT."
4. Edit the PLOT file and insert the mask level numbers as shown in Table 2. This mask level number is required to separate levels in the PLOT file.
5. The original Mann 1600 code will generate 10X reticles; therefore, the code needs to be reduced to 1X by the command "SI TCC221.PLT AS TCS221,PFL SCO.1."
6. Survey the TCS221.DFL File using "SURVEY TCS221,DTL L1." The results are shown in Table 3.
7. Generate a Versatec plotting tape using the survey command as shown in Table 4.
8. Plot checkplots and inspect them. Versatec plots of Levels 3 and 4 of TCS221 are shown in Figs. 1 & 2.
9. Generate DFL Tape from TCS221.DFL File by using the commands shown in Table 5.
10. Load the DFL Tape into the Applicon and convert the DFL to Applicon Graphix System Units.

    For Mann 1600 Tape 0.025 mil = 1 AGS unit

    MEBES Tape 0.02 mil = 1 AGS unit
11. Generate Technology File as shown in Table 6.
12. Generate MEBES tape using the Technology File.
13. Generate MEBES mask (master).
14. Make working plate from master.

TABLE 2. INSERTION OF LEVEL NUMBER IN TCS221.PLT FILE

```
LIST TCS221.PLT
 TCS221.PLT
00560    .................
00570    .................
00580 O X2540Y2617.5 R120 T40 L120 B40
00590 O X2660Y2617.5 R120 T40 L120 B40
00600 O X2779.45024Y2617.5 R30.49984 T40 L30.49984 B40
00610 O X1190Y3628.95008 R40 T28.5 L40 B28.5
00620 O X1975Y3290 R25 T10 L25 B10
00630 O X1999.95008Y3290 R24.5 T20 L24.5 B20
00640 O X1975Y3310 R25 T10 L25 B10
00650 ; "LEVEL 2 COMPLETE
00660 N 3
00670 ; "MSFC STAR LEVEL 3, POLY DEFINITION 1728 GATE CMOS SOS ARRAY
00680 ; "NEGATIVE DEVELOP 3X3 GLASS  S&R X=162.0 Y=131.0
00690 O X1975Y675.45 R25 T34.5 L25 B24.5
00700 O X1999.95008Y700 R24.5 T25 L34.5 B25
00710 O X1170Y1322.5 R120 T20 L120 B20
00720 O X1389.45Y1322.5 R50.5 T20 L50.5 B20
00730 O X1340Y1322.5 R120 T20 L120 B20
00740 O X1460Y1322.5 R120 T20 L120 B20
00750    .................
00760    .................
00770 O X1700Y1322.5 R120 T20 L120 B20
00780 O X1820Y1322.5 R120 T20 L120 B20
00790 O X1940Y1322.5 R120 T20 L120 B20
00800 O X1999.95008Y3290 R24.5 T20 L24.5 B20
00810 O X1975Y3310 R25 T10 L25 B10
00820 ; "LEVEL 3 COMPLETE
00830 N 4
00840 ; "MSFC STAR LEVEL 4, N+ DEFINITION 1728 GATE CMOS SOS ARRAY
00850 ; "POSITIVE DEVELOP 3X3 GLASS  S&R X=162.0 Y=131.0
00860 O X1703.5Y1467.45008 R17 T8.5 L17 B8.5
00870 O X1679.5Y1467.45008 R17 T8.5 L17 B8.5
00880 O X1655.5Y1467.45008 R17 T8.5 L17 B8.5
00890 O X1631.5Y1467.45008 R17 T8.5 L17 B8.5
00900    .................
00910    .................
READY
```

TABLE 3. SURVEY OF TCS221.DFL

```
READY
ART
◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆
#################################### 4 / 2 / 80 ####################################
            1. HELP IS NOW AVAILABLE FOR ART (SEE ARTNEWS)
◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆◆
CUR      ART    VERSION 12B    22:02:18     04/27/80

TSO◆SURVEY TCS221.DFL LI

SURVEY ENTERED VER. 12B

◆◆◆◆◆ NO ERRORS DETECTED

MASK LEVEL      # L'S      # P'S      # D'S      # E'S      # H'S      TOTAL

         3          0          0      14217          0          0      14217
         4          0          0       1733          0          0       1733
         5          0          0       3921          0          0       3921
         6          0          0       3287          0          0       3287
         7          0          0       1716          0          0       1716
         8          0          0       1999          0          0       1999
         9          0          0        130          0          0        130
        10          0          0       1767          0          0       1767
        11          0          0       3537          0          0       3537
◆◆◆◆◆TOTAL         0          0      32307          0          0      32307

       0 DEFINITIONS                                0 Q-CALLS

     TOTAL DFL SEGMENTS:       32353       TOTAL DFL WORDS:       161977

                        X                    Y
            MIN       20.0000              60.0000
            MAX      379.9998             339.9998

SURVEY COMPLETED
```

TABLE 4. COMMANDS FOR VERSATEC CHECKPLOT TAPE

```
TSO*BATCH

BATCH*PI UE

BATCH*SCALE 200

BATCH*UFR 20,60,380,340

BATCH*CH TC9821.DFL 382:4815:581:690:781:20:8619:9920:1095:1193 E

BATCH*SUB PP

--CLASS-=-H----------------------------------------------------------

CPU TIME IN MINUTES = 20
PLEASE TYPE VERSATEC TAPE NAME (6 CHARACTERS)
A0809 9 «9
JOB RCA78SH(JOB05132) SUBMITTED

TSO*QU
READY.
ST
JOB RCA78SH(JOB05132) WAITING FOR EXECUTION, IN HOLD STATUS
READY
LOGOFF
RCA78S LOGGED OFF TSO AT 23:44:09 ON APRIL 27, 1980
```

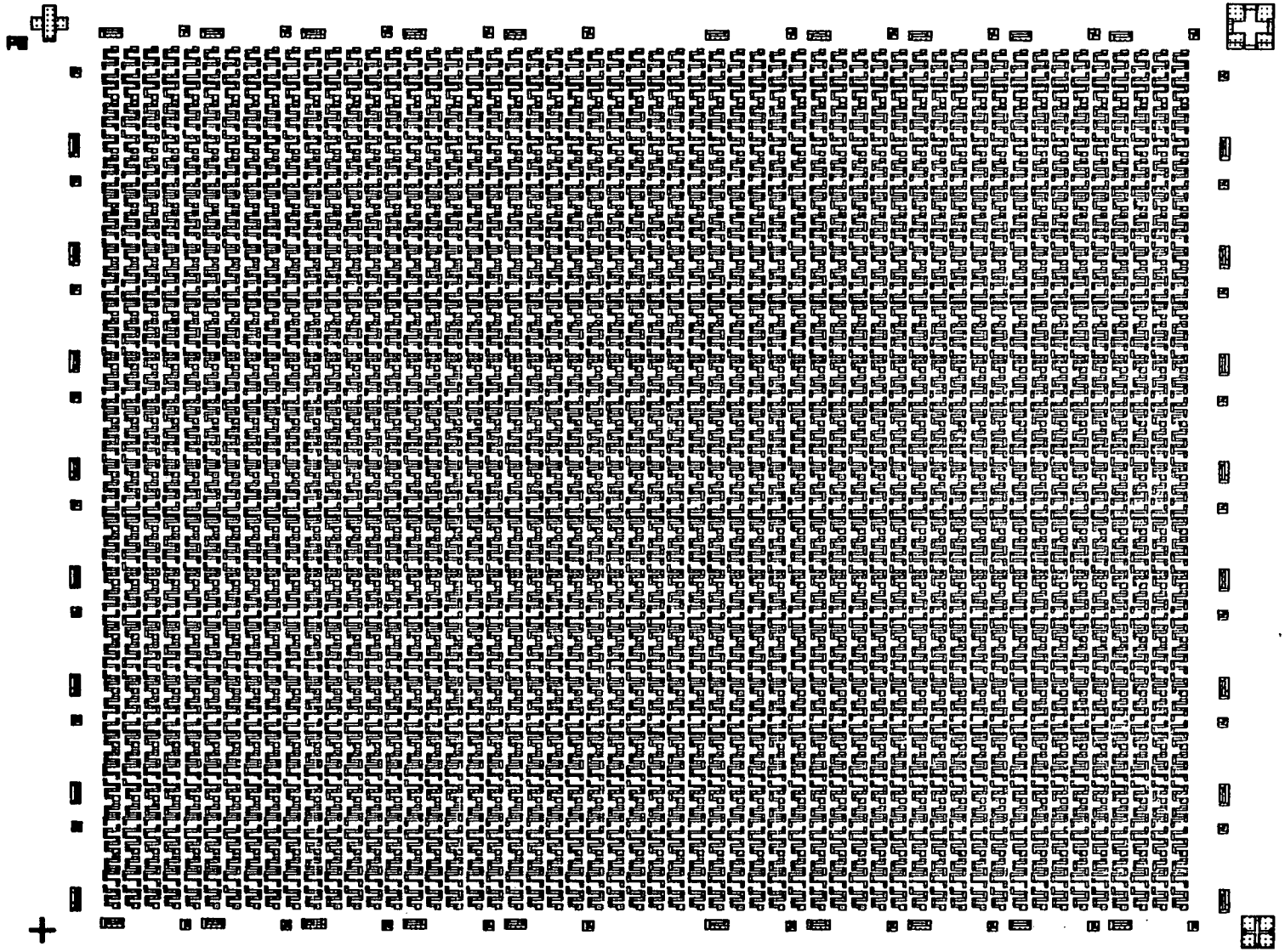

Figure 1. Versatec checkplot of TCS221 polysilicon level (L-3).

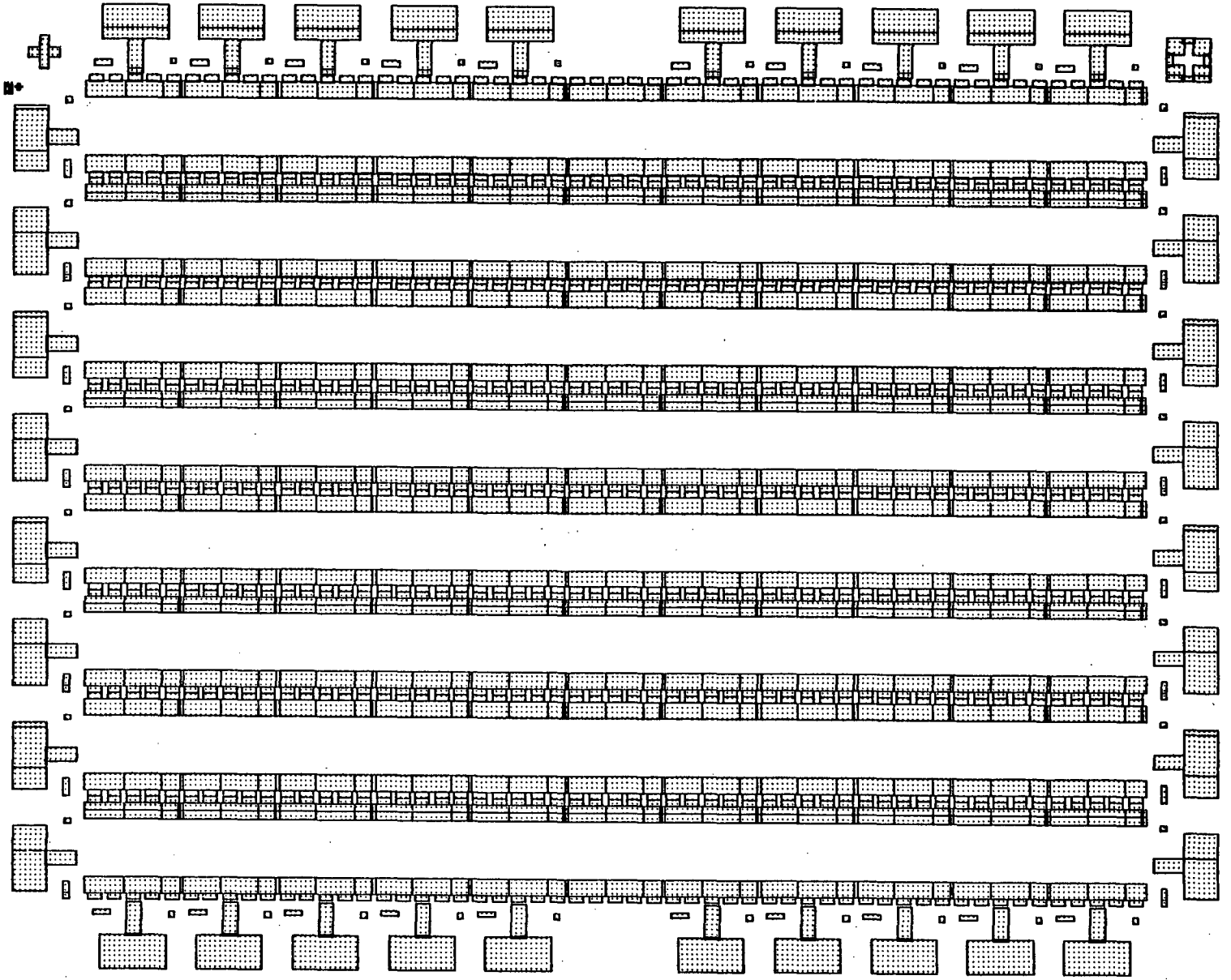

Figure 2. Versatec checkplot of TCS221 N+ diffusion level (L-4).

TABLE 5. COMMANDS TO GENERATE DFL TAPE FROM IBM370 TSO FILE

```
ART
**************************************************************************
########################## 4 / 2 / 80 ##########################
          1. HELP IS NOW AVAILABLE FOR ERT (SEE ERTNEWS)
**************************************************************************
OUR     ERT   VERSION 122   23:08:07    04/27/80

TSO*ZA

BATCH*SIFT TCS221.DFL AS MT:1

PLEASE TYPE THE TAPENAMEA00175

BATCH*SUB FF

CLASS = O

OTHER = U

CPU TIME IN MINUTES = 1
JOB RCA7850(JOB05109) SUBMITTED

TSO*QUIT
READY
```

TABLE 6. TECHNOLOGY FILE OF TCS221 WITH TCS148 INSERT TEST CHIP

```
TCS221.TECHFILE.DATA
     PRODUCT LINE: SOS
     PRODUCTION TYPE: CONTACT
     P.G. TYPE: ETEC
     MASK SIZE: 4
     S&R MASK INSP: OA
     PROD MASK INSP: TS
     PROD MASK MAT:  3,L 4,L 5,L 6,L 7,L 8,L 9,L 10,L 11,L
     GEOMETRY: POSITIVE
     LEVEL NAME: 3,POLY 4,N+ 5,CNT 6,MET1 7,VIA 8,MET2 $
     9,PAD 10,P+ 11,ILDS
     GRID: 3,N 4,N 5,Y 6,N 7,Y 8,N 9,Y 10,N 11,N
     PROD MASK AMT: 3,2 4,2 5,2 6,2 7,2 8,2 9,2 10,2 11,2
     DIAG KEY 1 LEV: 3,3 4,4 5,5 6,6 7,7 8,6 9,7 10,9 11,8
     CHIP UNITS: MILS
     WAFER SIZE: 3
     WAFER GEOMETRY: CIRCLE
     CHIP ADDRESSING: HALF MICRON
     PATTERN GENERATOR SCALE: 1
     TONE: 3,- 4,+ 5,+ 6,- 7,+ 8,- 9,+ 10,+ 11,-
     DROP OUT CODE: 4
     DIAG KEY 1 NAME: TCS148ZB
     BORDER OVERLAP: 0.0
     RUNOUT: 0,0
```

III. PROCESS

A. PROCESSING OF MSFC SC102

Three lots each of silicon-gate CMOS/SOS and aluminum-gate COS/MOS bulk silicon were processed using the all-ion-implantation process* developed under this same contract. All wafers were processed to the point of the first-level metallization. Aluminum was patterned on two control wafers from each lot. The wafers were alloyed, and before shipment to NASA, a Wafer Acceptance Test (WAT) was performed to verify that every processing step was done properly. A sample of the WAT report is given in Table 7.

B. DELIVERY

Twenty-nine 3-in. wafers of TCS221 and forty-two 3-in. wafers of TCC261 were delivered to MSFC along with master plates of the MEBES mask set and working plates.

*D. S. Woo, "Characterization of Silicon-Gate CMOS/SOS Integrated Circuits Processed With Ion Implantation," Final Report prepared for Marshall Space Flight Center under Contract No. NAS8-31986, May 1980.

TABLE 7. WAFER ACCEPTANCE TEST DATA OF LOT S3001

WO# EØ12-1767 N.A.S.A. (D.WOO)

INDIVIDUAL-LOT ANALYSIS (SOS)

LOT=S3ØØ1 TYPE=TCS221 PROC =SKNI1 RCA
DATE=Ø9/Ø4/8Ø-11/Ø4/8Ø #CHIP= 2 SSTC

		N-CHANNEL				P-CHANNEL			
		L=4um	5um	6um	7um	4um	5um	6um	7um
TR1	Vt (V,ØA)	Ø.65	Ø.78	Ø.82	Ø.87	Ø.71	Ø.78	Ø.86	Ø.93
	Idss (nA)	Ø.ØØ	51.31	3Ø.34	11.47	24.8Ø	19.55	5.72	5.63
	BVds (V)	1Ø.24	17.13	2Ø.44	23.65	24.27	28.48	29.83	3Ø.74
	K (uA/V2)	167.28	113.32	9Ø.8Ø	73.85	135.39	9Ø.31	69.Ø2	55.42
	ID(mA,G5.D5)	2.66	1.79	1.46	1.19	2.35	1.62	1.18	Ø.95
	ID(mA, 5,1Ø)	3.73	2.45	1.97	1.53	2.68	1.78	1.3Ø	1.Ø4
	ID(mA,1Ø, 5)	6.94	5.2Ø	4.44	3.73	6.79	5.Ø4	3.71	3.28
	ID(mA,1Ø,1Ø)	8.16	6.14	5.27	4.45	8.Ø4	5.99	4.46	3.95
	Kn/Kp: Vn+Vp	2.49	2.54	2.64	2.66	1.35	1.56	1.69	1.8Ø
TR2	Vt (V,ØA)	Ø.86	Ø.87	Ø.86	Ø.84	Ø.91	Ø.94	Ø.99	Ø.95
	Idss (nA)	6.72	3.94	5.54	2.86	4.15	3.13	3.88	2.38
	K (uA/V2)	11Ø.96	87.11	73.57	62.38	86.36	67.29	55.Ø7	47.76
	ID(mA,G5,D5)	1.91	1.48	1.26	1.Ø6	1.63	1.23	Ø.97	Ø.84
	ID(mA, 5,1Ø)	2.42	1.79	1.48	1.23	1.76	1.3Ø	1.Ø2	Ø.87
	ID(mA,1Ø, 5)	6.18	4.38	4.13	3.54	5.66	4.39	3.57	3.Ø6
	ID(mA,1Ø,1Ø)	7.39	5.91	5.Ø4	4.31	6.83	5.37	4.39	3.79
	Kn/Kp: Vn+Vp	2.57	2.58	2.66	2.59	1.77	1.82	1.85	1.79
	RO(ns: XYLD)	1.58	1.85	2.91	3.87	5Ø.ØØ	1ØØ.ØØ	1ØØ.ØØ	5Ø.ØØ

LN1=L LN2=2L LP1=L LP2=2L
WN1=5Øum WN2=1ØØum WP1=1ØØum WP2=2ØØum

			AVG	STDV	#WC
BVox (V)		NMOS	49.69	15.66	8
		PMOS	55.3Ø	13.24	8
METAL STEP COVERAGE (Ohm)					
1ØØ-Sq METAL + 44 STEPS			2.33	Ø.26	8
.66Rc+56Rs(POLY) (k-Ohm)			3.44	1.17	8
FOR POLY-METAL Rc(5um X 1Øum)					
Rs (Ohm/Sq)		NMOS-DS	76.18	2.78	8
at 1mA		PMOS-DS	38.67	2.44	8
		NMOS-POLY	445.64	38.57	8
		PMOS-POLY	5Ø.32	1.78	8
Rc-Coeff		NMOS-DS	1.11	Ø.Ø7	8
(1ØuA/1mA)		PMOS-DS	1.ØØ	Ø.ØØ	8
		NMOS-POLY	1.ØØ	Ø.ØØ	8
		PMOS-POLY	1.ØØ	Ø.ØØ	8
GATED-DIODE		FWD at 1ØØuA (V)	1.65	Ø.19	7
TO Vss		REV at 1ØuA (V)	25.99	4.13	7
GATED-DIODE		FWD at 1ØØuA (V)	1.21	Ø.Ø5	8
TO Vdd		REV at 1ØuA (V)	3Ø.54	1.31	8
ZENER-DIODE		REV1 at 1ØuA (V)	23.32	2.15	8
5-STACK		REV2 at 1ØuA (V)	23.53	2.11	8

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15. Supplementary Notes

16. Abstract

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